Microprocessor with Branch Control Apparatus

FIG. 1

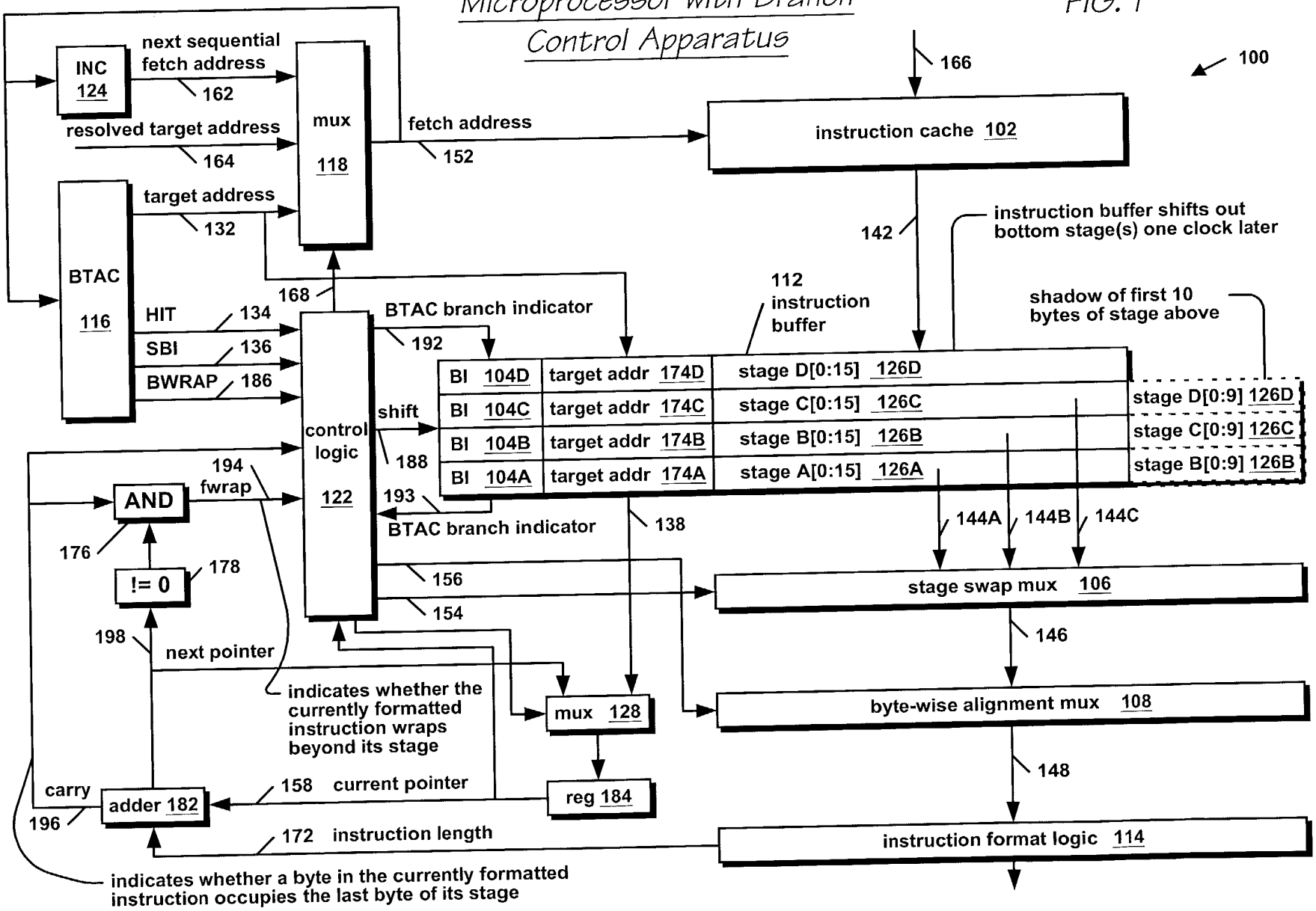


FIG. 2

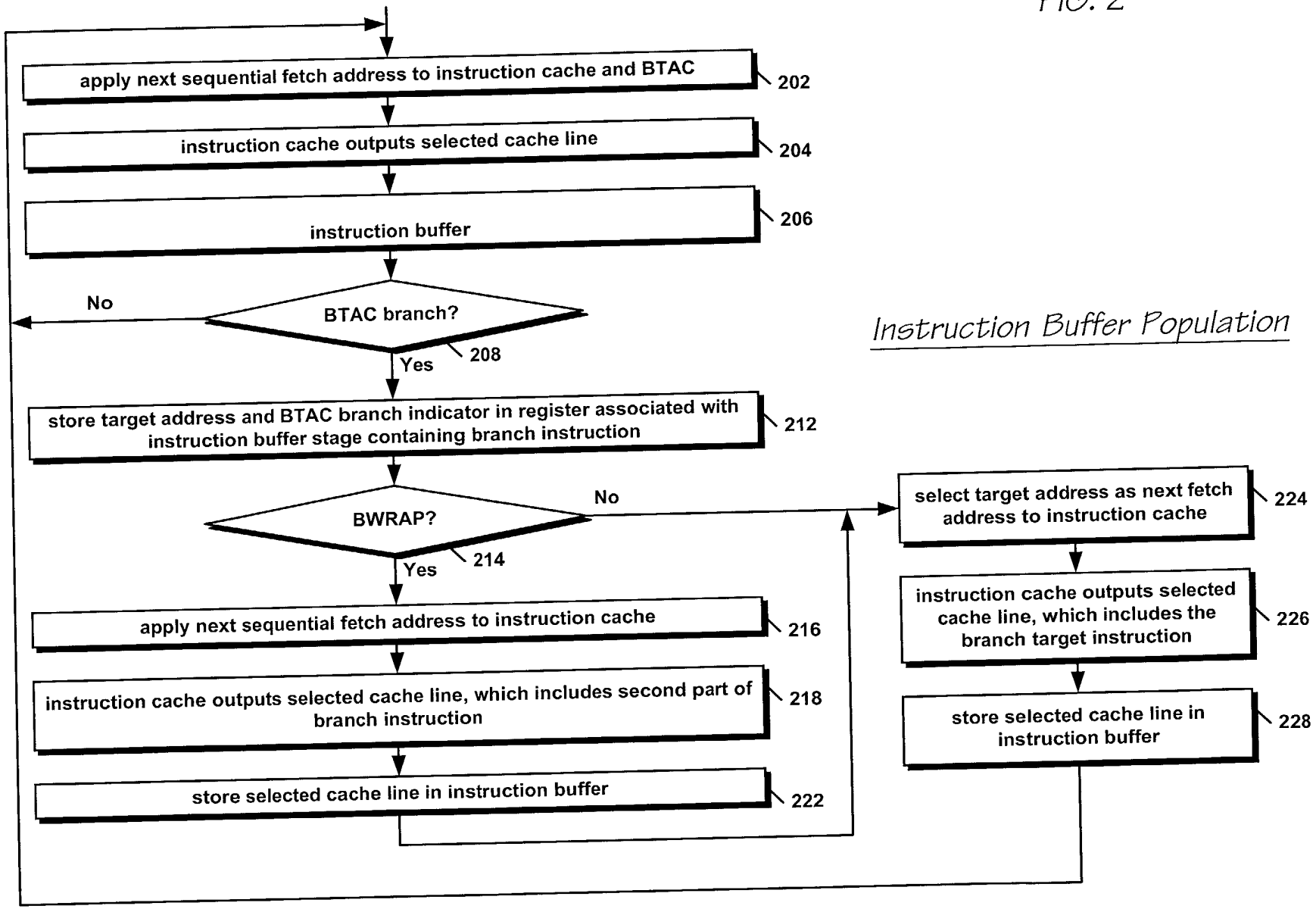
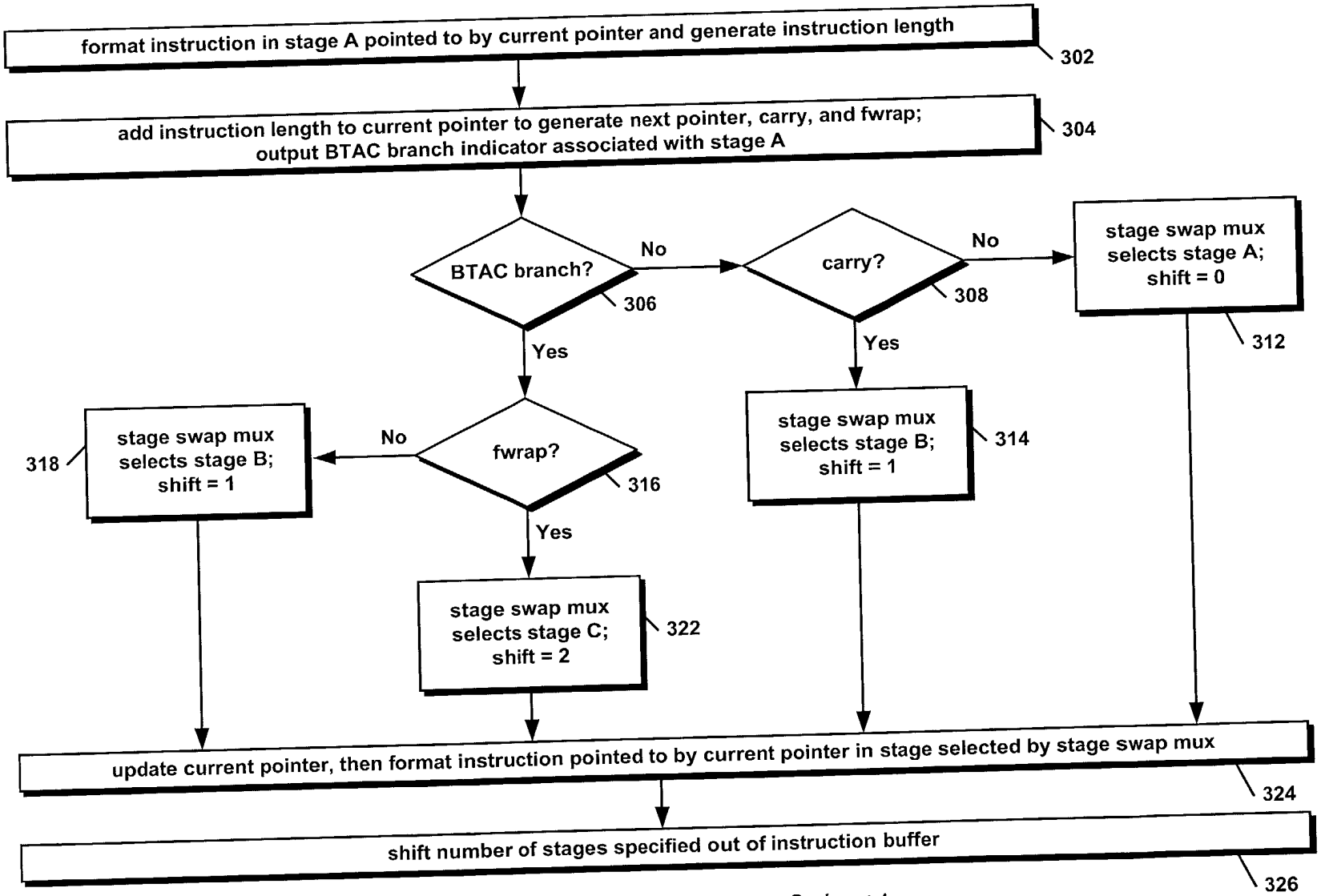
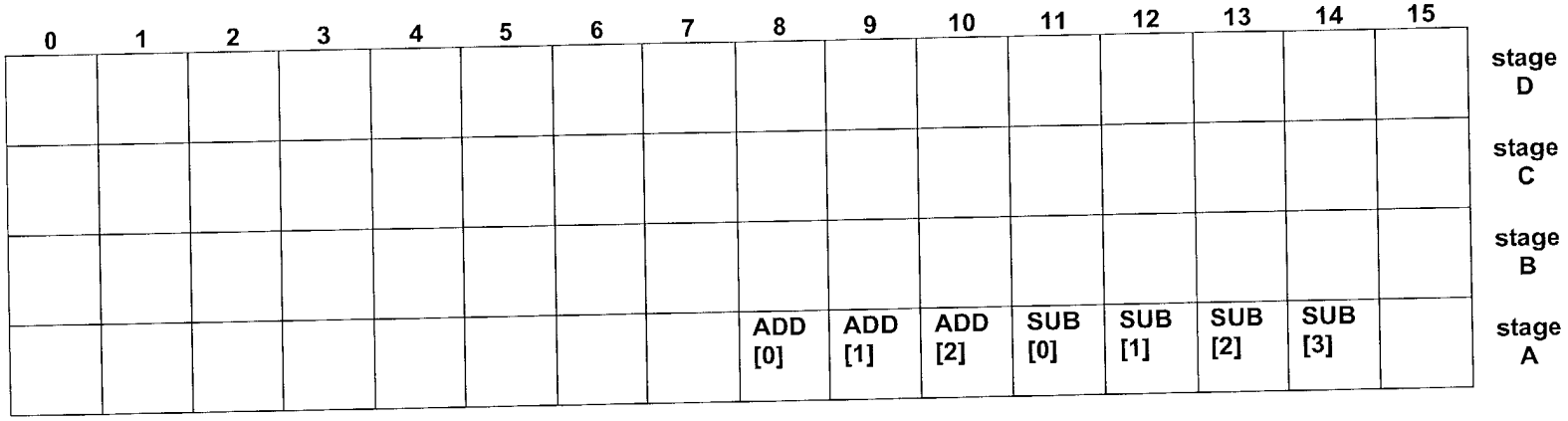

apply next sequential fetch address to instruction cache and BTAC
202
instruction cache outputs selected cache line
204
instruction buffer
206
BTAC branch?
208
No
Yes
store target address and BTAC branch indicator in register associated with instruction buffer stage containing branch instruction
212
BWRAP?
214
No
Yes
apply next sequential fetch address to instruction cache
216
instruction cache outputs selected cache line, which includes second part of branch instruction
218
store selected cache line in instruction buffer
222
select target address as next fetch address to instruction cache
224
instruction cache outputs selected cache line, which includes the branch target instruction
226
store selected cache line in instruction buffer
228
Instruction Buffer Population

FIG. 3



Instruction Buffer Stage Selection

Figure 4A



current pointer = 8
instruction length = 3
BTAC branch indicator = false
target address[0:3] = n/a

next pointer = 11
carry = false
fwrap = false

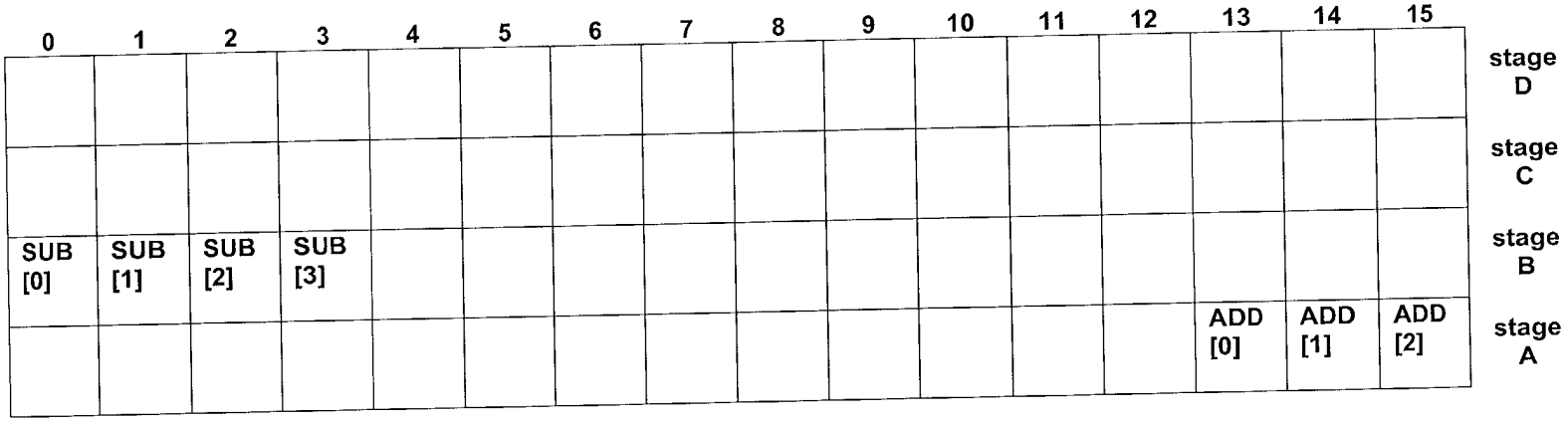
stage swap mux selects stage A

shift = 0

112

Instruction Buffer Stage Selection Example: Case 1

Figure 4B



current pointer = 13
instruction length = 3
BTAC branch indicator = false
target address[0:3] = n/a

next pointer = 0
carry = true
fwrap = false

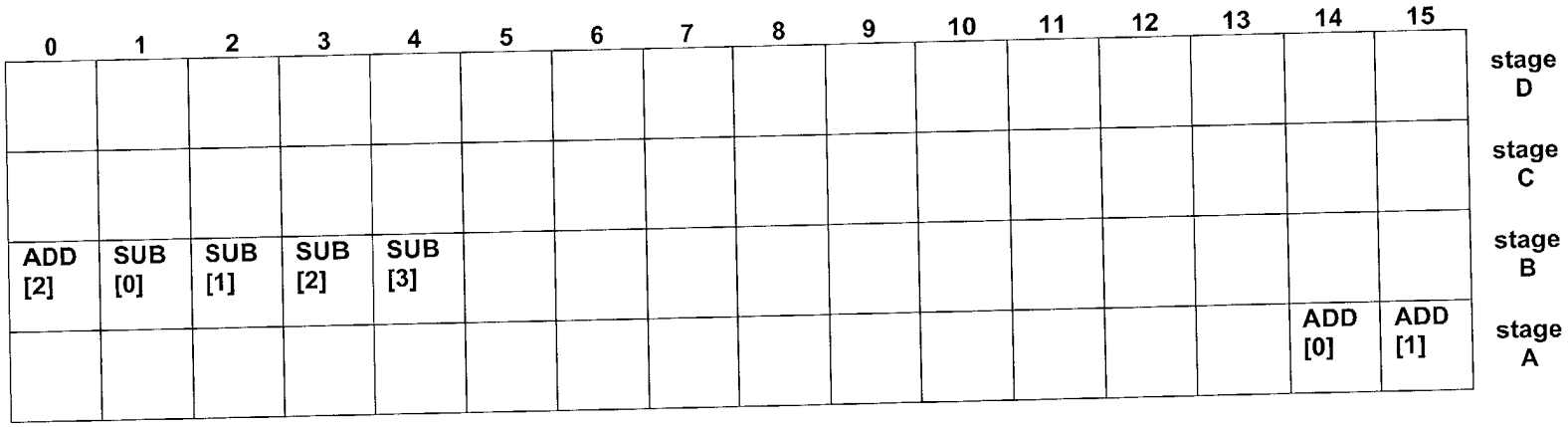
stage swap mux selects stage B

shift = 1

112

Instruction Buffer Stage Selection Example: Case 2

Figure 4C



current pointer = 14
instruction length = 3
BTAC branch indicator = false
target address[0:3] = n/a

next pointer = 1
carry = true
fwrap = true

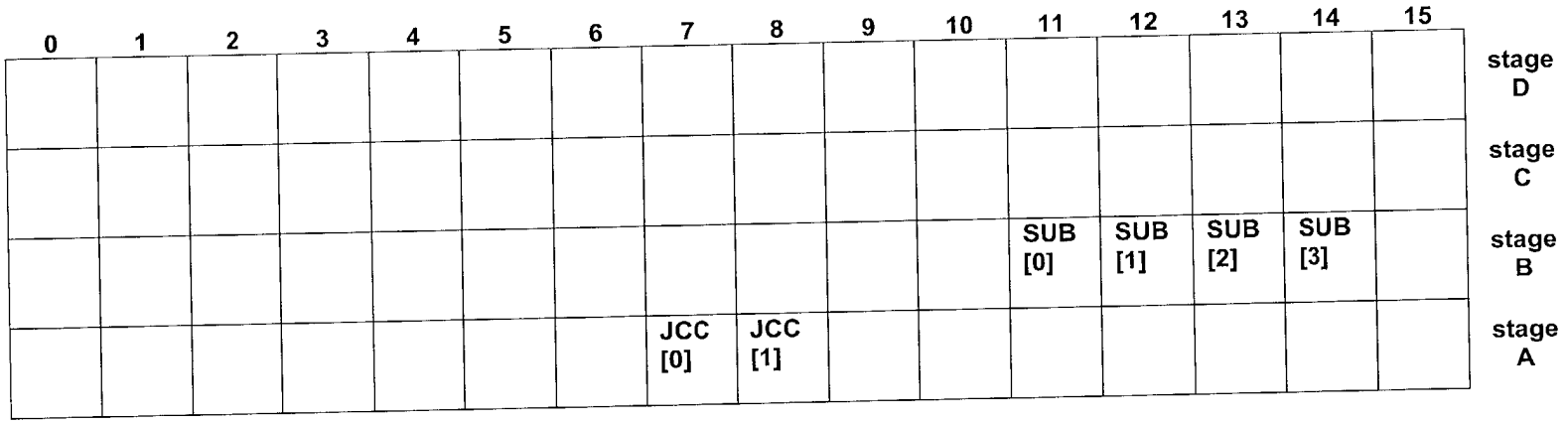
stage swap mux selects stage B

shift = 1

112

Instruction Buffer Stage Selection Example: Case 3

Figure 4D



current pointer = 7
instruction length = 2
BTAC branch indicator[7] = true
target address[0:3] = 11

next pointer = 9
carry = false
fwrap = false

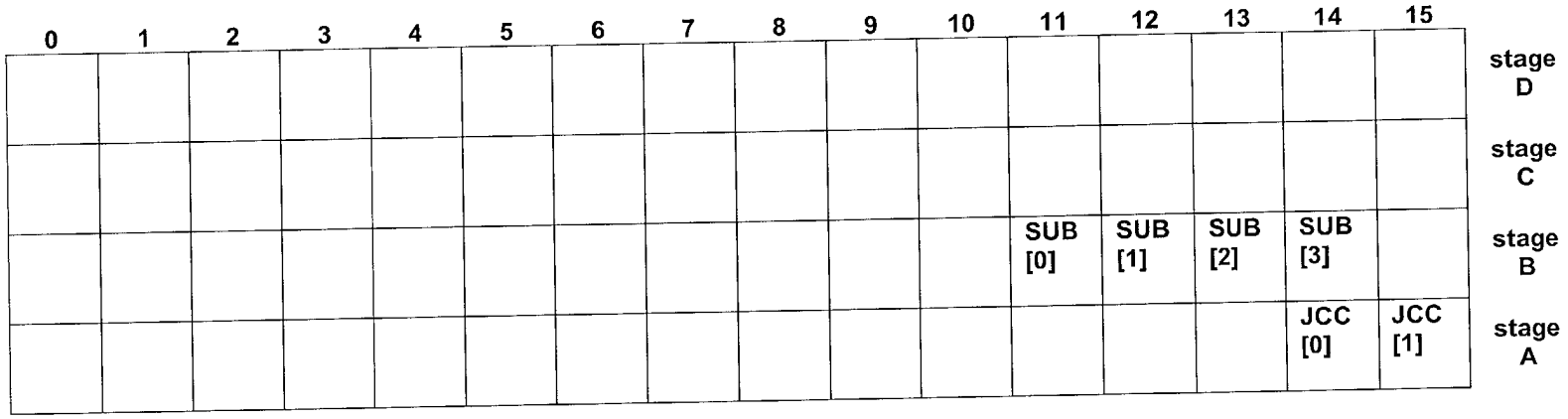
stage swap mux selects stage B

shift = 1

112

Instruction Buffer Stage Selection Example: Case 4

Figure 4E



current pointer = 14
instruction length = 2
BTAC branch indicator[14] = true
target address[0:3] = 11

next pointer = 0
carry = true
fwrap = false

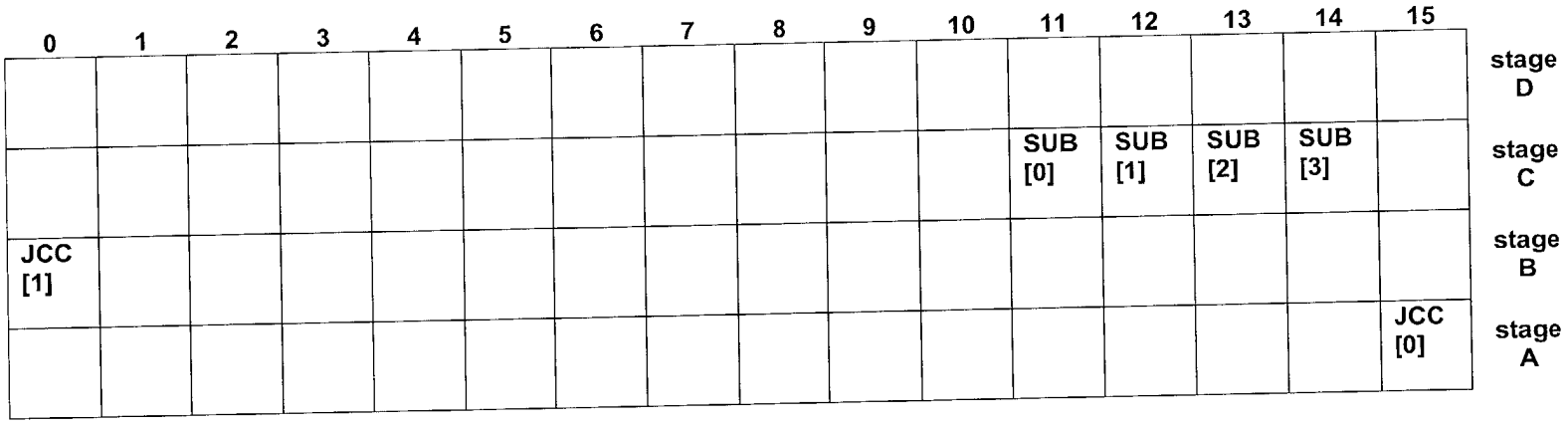
stage swap mux selects stage B

shift = 1

112

Instruction Buffer Stage Selection Example: Case 5

Figure 4F



current pointer = 15
instruction length = 2
BTAC branch indicator[15] = true
target address[0:3] = 11

next pointer = 1
carry = true
fwrap = true

stage swap mux selects stage C

shift = 2

112

Instruction Buffer Stage Selection Example: Case 6